genesys ideation

Harrier-F VDK

User's Manual

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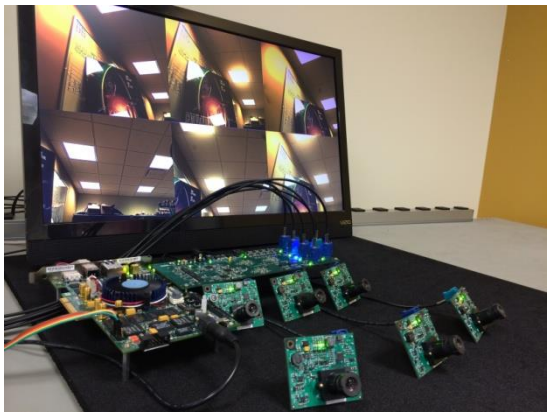
Harrier-F VDK

User's Manual

1 Introduction

1.1 Overview

The Genesys Ideation Harrier-F Video Development Kit (VDK) is a multiple camera daughter card solution for Altera's developer kits. The VDK can be used to develop products for the automotive, industrial, and security industries. Automotive industry trends suggest a need for multiple cameras in a vehicle to assist the driver with safety related features. Automation incorporating machine vision has been a consistent trend in the Industrial business sector. Certain security concerns can be addressed with multiple camera systems utilizing an intelligent computational platform near the video source.



1.2 Features

A complete VDK has the following features:

- Altera FPGA with Nios II or HPS
  - Use with any Altera development kit with a standard HSMC interface
- Up to 8 camera inputs
  - 6 continuous inputs and 2 multiplexed inputs
  - Developed to use the Finch Imager
- Texas Instruments FPD-Link III deserializer transport interfaces
  - Coaxial cable interface
  - Camera power supplied by Harrier daughter card
  - High Speed pixel data (up to 1.4Gbps)
  - Remote I/O for exposure control
  - Up to 15m coaxial cable connection
- FAKRA coaxial interconnect
  - Positive locking coaxial
- Reference design in programmable logic and software
  - Platform setup
  - Image capture
  - Image display

1.3 System Block Diagram

The system block diagram describing the interfacing between the Fincher Imagers, Harrier Daughter Card, and Altera Development kit is shown below. Each of the Finch Imagers connects to and draws power from the Harrier Daughter Card via the FPD-Link III serial interface. The Harrier Daughter Card mates directly to the Altera Development Kit via a built-in High-Speed Mezzanine Card (HSMC) connector.

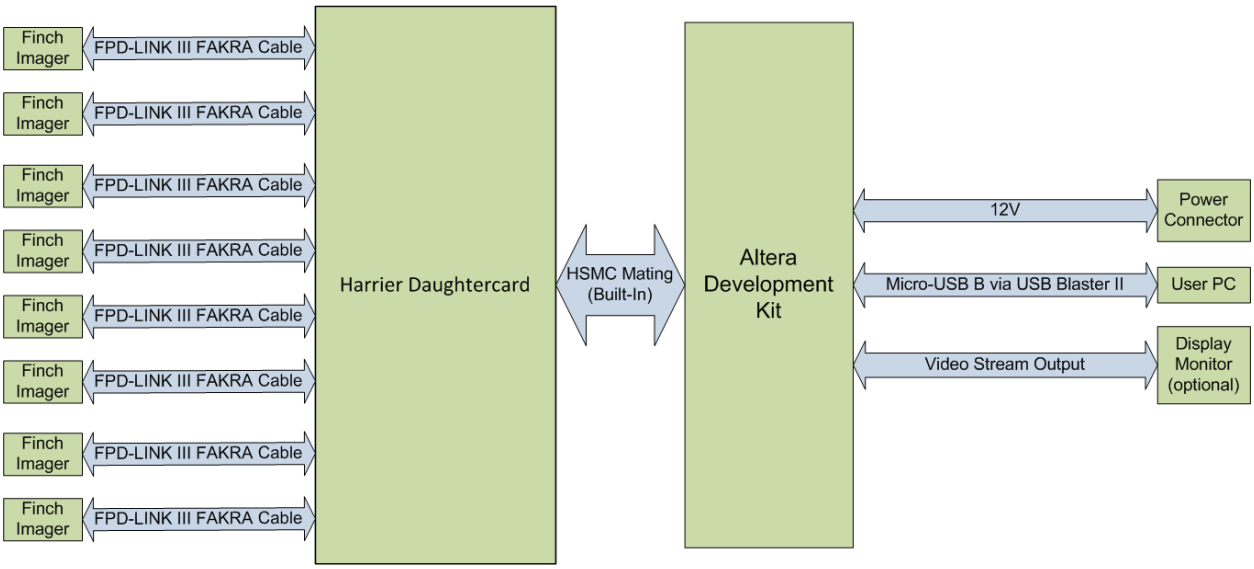


Figure 1-1: Harrier F VDK System Block Diagram

The Harrier daughter card accommodates multiple imagers (1280 x 720 @ 60 fps) and transports the pixel data via the Texas Instruments FPD-Link III interfaces for each independent video path. Connection between imagers and daughter card is accomplished by a coax cable using the FAKRA interconnect system. The platform also includes software and custom logic reference design to enable the developer to quickly realize design goals beyond platform setup, image capture, and image display.

2 Getting Started

2.1 Kit Components

The following tables detail the components of the system:

Table 2-1: Harrier-F VDK Components

Harrier Daughter card	See detail below
Finch Imager (8)	See detail below
FPD-Link III Cable (8)	Coaxial cable for transmission of the FPD-Link III data for each imager.
HDL Configuration	Initialize imagers, clock video data in for each video stream, allow user I/O to control exposure or illumination on the CMOS imager board.
Software	System control and initialization, runs on Nios II microcontroller

	Initializes imagers (default) to 1280 x 720 @ 60 fps.

2.1.1 Altera Evaluation Board

The demonstration CL and SW are targeted for the Stratix IV-GX development kit.

2.1.2 FPD-Link III SMB Interconnect

The system utilizes a coaxial cable for transmission of the FPD-Link III data for each imager. There are SMB connectors with a FAKRA interconnect system on both the Finch and Harrier boards.

2.1.3 Harrier Daughter Card

The Harrier Card accepts up to 8 video signals, streamed over multiple FPD-Link III interfaces and converts them back into parallel data. However, only 6 continuous streams of video are available simultaneously. The multiplexed inputs can be programmatically switched at run-time to allow 2 alternative video streams to be manipulated and displayed. Once the high speed bit stream is converted to parallel data, the signals will be routed through the HSMC connector and to the FPGA The data is then sent through a video pipeline in the FPGA where the demonstration program software can manipulate the video streams for output.

2.1.4 Finch Imager Board(s)

The CMOS Imager Board uses the Aptina AR0132AT HD imager as the source of the video data. The imager is initialized by the software for 60 frames of video data per second and 10-bit pixel data depth.

2.1.5 HDL Configuration

The custom logic used in the Cyclone FPGA initializes the imagers, clocks the video data in for each video stream, and allows user I/O to control exposure on the CMOS imager board. The reference design leverages several IP cores from Altera's Video IP Suite. A Nios II microcontroller is implemented to manage the initialization and control of the video streams.

2.1.6 Software

The software running on the Altera development kit is the main source of system control and initialization. The software will be available for development as a time limited binary library. This will allow the demonstrator and the developer to get a flavor of how to use and manipulate the demonstration software to expand its functionality. A Nios II microcontroller is implemented on the FPGA to manage the initialization and control of the video streams.

2.2 Setup

2.2.1 Finch to Harrier Connection

Locate the FPD-Link III connector on the Finch Imager board, as highlighted in the figure below.

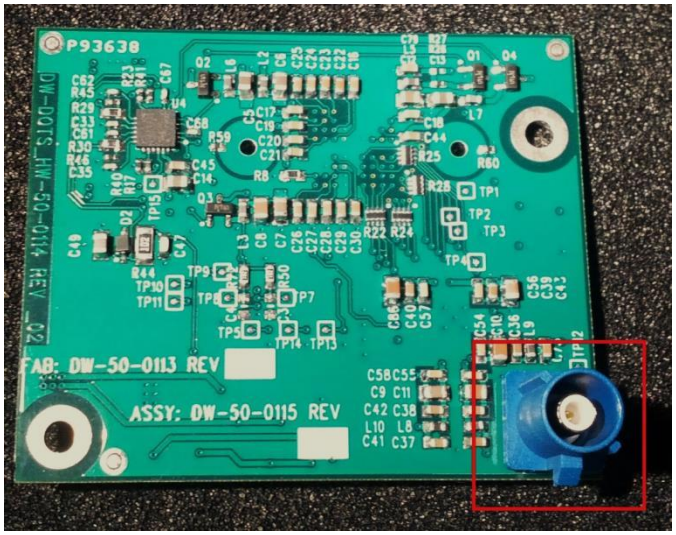
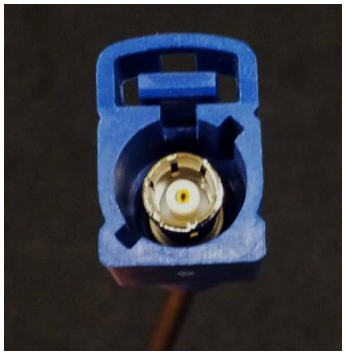
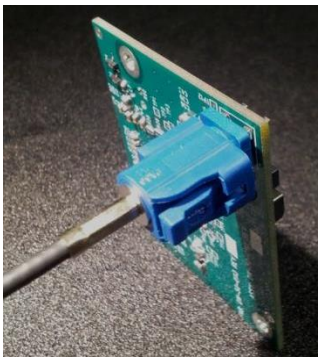


Table 2-3: Finch Imager

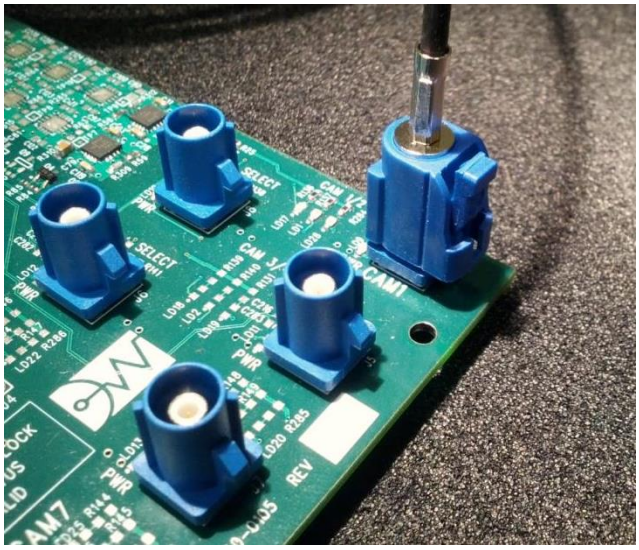
Align the slotted connector housing on the cable with the keys on the Finch board and snap into place.





Next, locate the connector associated with the desired data channel on the Harrier Daughter card.

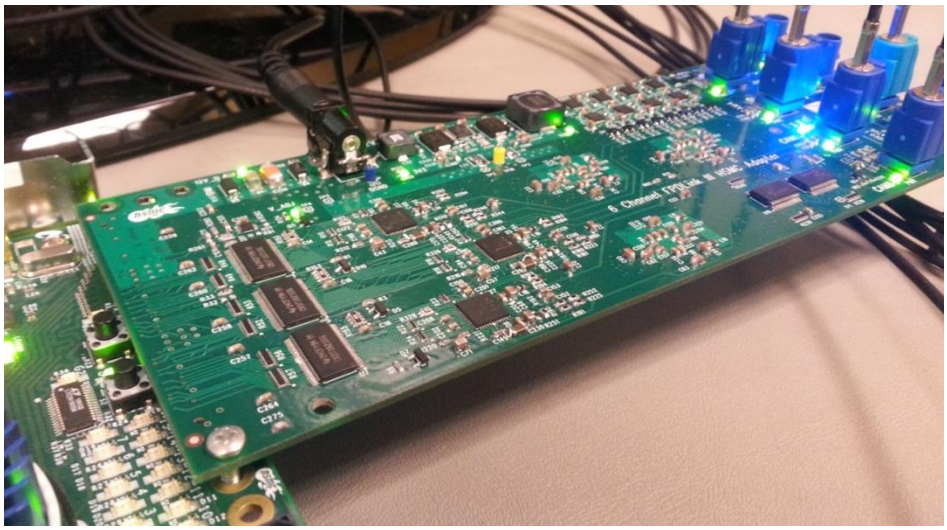
Again, align the slotted connector housing on the cable with the keys on the Harrier board and snap into place.



Again, align the connector Harrier Deserializer with the keys on the Finch and Harrier boards and snap into place.

2.2.2 Harrier to FPGA Connection

The Harrier Daughter card connects to the FPGA via the built in HSMC connector. 5mm spacers between the two boards are recommended, as well as stand-offs on the opposite end of the Harrier card.



2.2.3 Powering the Harrier Daughter Card

There are two options for powering the Harrier Daughter Card. Note that 12V will be passed to the Harrier card from the Altera Dev Kit via the HSMC connector. Alternatively, the board can be powered with 12V from a DC barrel jack (i.e. J1).

2.2.4 Powering the Finch Imager

Power will be supplied to the Finch Imager from Harrier Daughter card via the FPD-Link III cable. Each imager is powered off by default until software enables the respective power switch.

2.2.5 FPGA Connections

Connect the power, USB, and display monitor cables to the FGPA. Refer to the manual for your chosen FPGA Dev Kit for specific instructions.

2.3 Power Up

When the Harrier Daughter card is properly powered (see Section 2.2.3 above), four status LEDs should be illuminated. LD1 signifies that the 12V regulator is working correctly. LD2 corresponds to the VADJ_D regulator, LD3 to the 3.3V regulator, and LD4 to the 1.8V regulator.

2.4 Load Your First Project

After connecting the system together (see Sections 2.2.1 and 2.2.2 above), you are ready to load the FPGA with a configuration and software. The following steps explain how to run the demonstration software ELF file and how to program the FPGA with the demonstration SOF. The demonstration will configure the cameras, initialize the video pipelines, and tile all 6 streams of video on the HDMI output. The demonstration configuration and software can be found on the respective product pages on the Genesys Ideation web site (genesysideation.com).

3 For more information

3.1 Genesys Ideation Reference Manuals

For more information on the Harrier Daughter Card and Finch Imager, please visit our web site (http://www.genesysideation.com/support) for their specific reference manuals.

3.2 Altera Development Boards

The Harrier-F VDK was developed with the Stratix IV GX Development Board. However, the VDK can be used for development with any development board that follows the HSMC standard. It does not use high speed transceivers on this development board for any of the camera I/O. For more information on the Stratix IV GX Development Board, please visit Altera's web site (http://www.altera.com/products/devkits/altera/kit-siv-gx.html) for specific reference manuals.

4 Programmable Logic Reference

4.1 Key Features

The Harrier-F VDK was developed with the Stratix IV GX Development Board. As such, the programmable logic reference utilizes some of the features from this development board. The subsequent bullet list details some of the more notable features in the logic reference design:

- NIOS-II 32-bit RISC Processor
- Six parallel video pipelines
- I2C interface for serdes control, camera configuration, and I/O expansion
- Software controllable video pipeline
- DDR3 memory interface
- HDMI output at 1920x1080 resolution at 60fps

The programmable logic reference is limited to 30 minutes run-time. If you are interested in further enhancement of the programmable logic reference or wish to have port to a different FPGA platform, please contact us at sales@genesysideation.com.

4.2 HDL Block Diagram

The following block diagram highlights the various sections of the FPGA configuration.

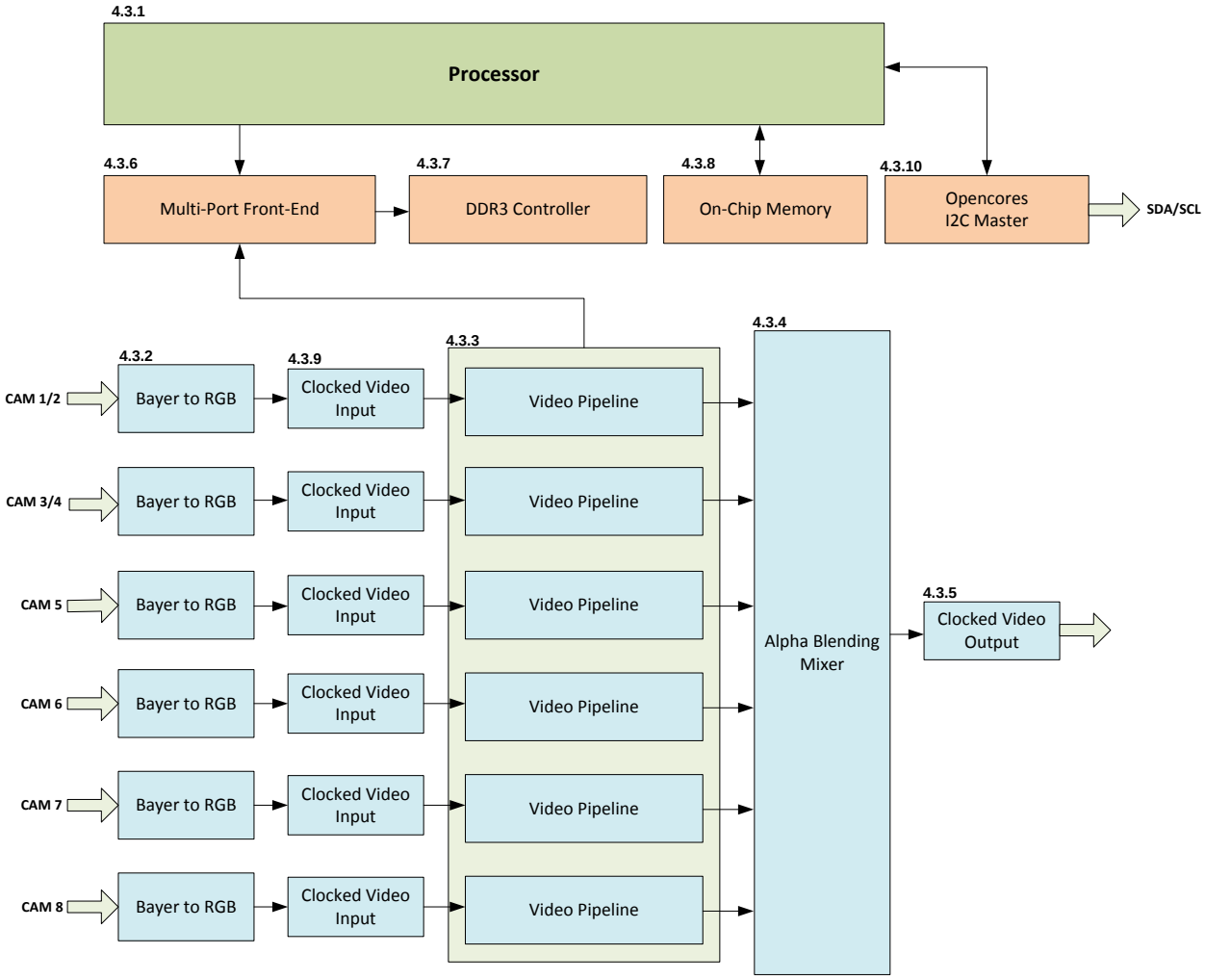


Figure 4-1: High-Level Multi-Camera Custom Logic Design

5 Software Reference

5.1 Key Features

The demonstration software available on the Genesys Ideation website performs the following functions:

- I2C configuration of the TI FPD-Link III serdes
- I2C configuration of the Aptina AR0132 CMOS Imager
- I2C controlled I/O Expander used for

  - Imager power control
  - Locked link indication
  - Alternate channel selection
- I2C configuration of the Krontel HDMI interface
- Pipeline configuration and manipulation
- UART interface for debugging and demonstration

This demonstration software was written for the Stratix IV GX Development Board. If you are interested in a port of the software to a different platform, please contact sales@genesysideation.com.

5.2 SW Block Diagram

The block diagram of the demonstration software is as follows:

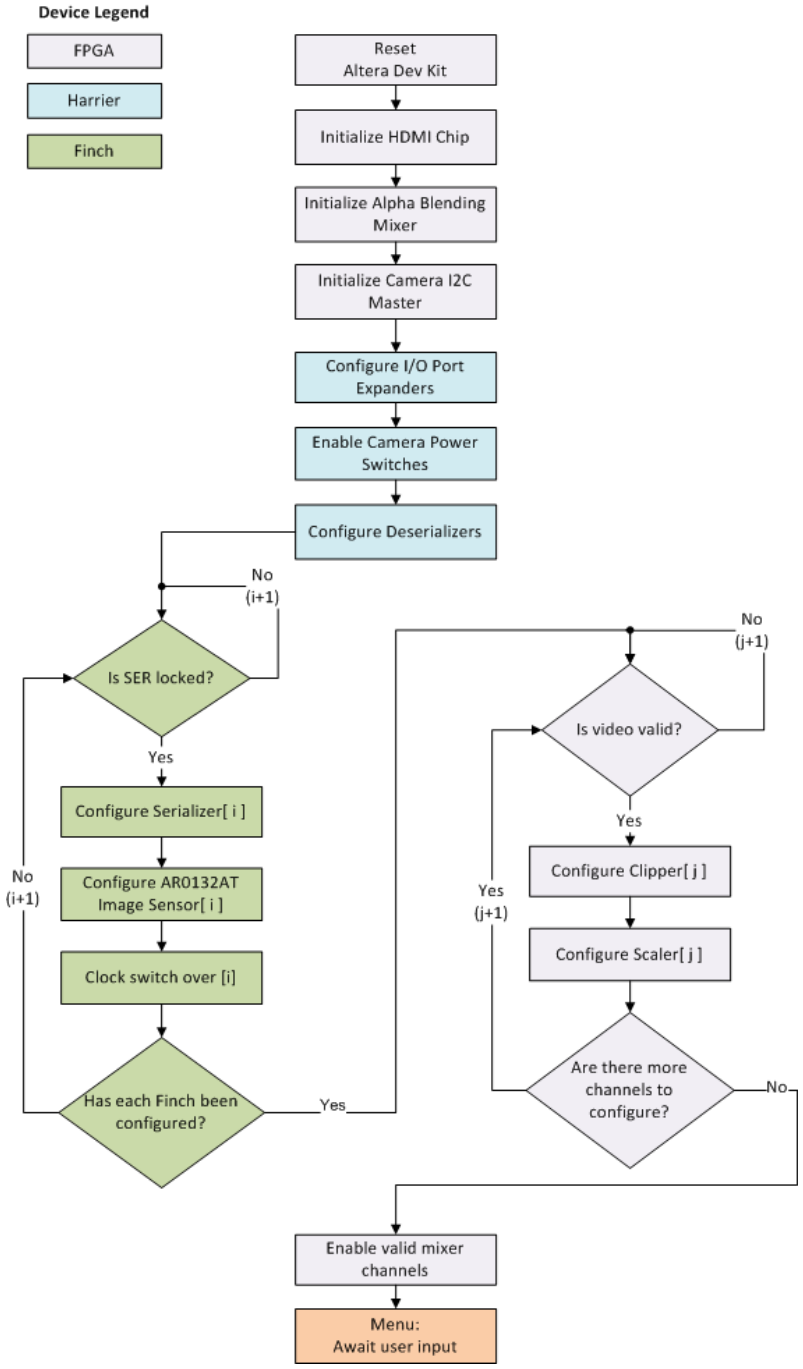


Figure 5-1: High-Level VDK Software Algorithm

5.3 Software Development Guide

The following section includes relevant information for software developers interested in writing custom drivers for the Harrier daughter card and the Finch camera boards.

5.3.1 Harrier Devices

The Harrier daughter card contains the following devices that are controlled via I2C:

- Microchip MCP23017 IO Port Expanders
- Texas Instruments DS90UB914Q FPD-Link III Deserializers

Please reference the “Harrier Daughter Card User Manual” for details on the developing software for the Harrier Daughter Card.

5.3.2 Finch Devices

The Finch board contains the following devices that are controlled via I2C:

- Texas Instruments DS90UB913Q FPD-Link III Serializers

Please reference the “Finch Imager User Manual” for details on the developing software for the Finch Imager.